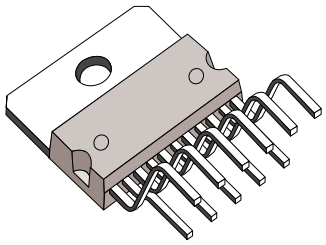
SGS-THOMSON MICROELECTRONICS

TDA1675A

VERTICAL DEFLECTION CIRCUIT

- SYNCHRONISATION CIRCUIT
- ESD PROTECTED
- PRECISION OSCILLATOR AND RAMP GENERATOR
- POWER OUTPUT AMPLIFIER WITH HIGH CURRENT CAPABILITY
- FLYBACK GENERATOR
- VOLTAGE REGULATOR
- PRECISION BLANKING PULSE GENERATOR
- THERMAL SHUT DOWN PROTECTION
- CRT SCREEN PROTECTION CIRCUIT WHICH BLANKS THE BEAM CURRENT IN THE EVENT OF LOSS OF VERTICAL DEFLECTION CURRENT



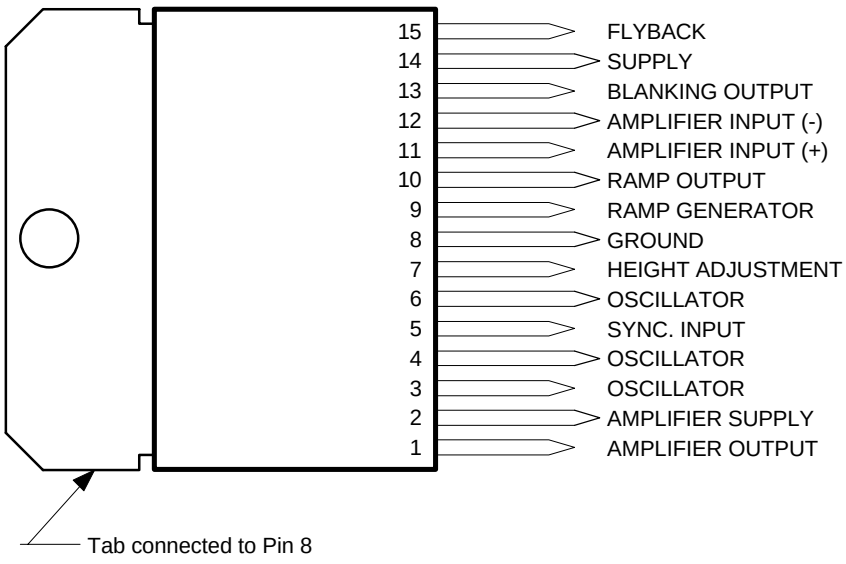
MULTIWATT 15
(Plastic Package)

ORDER CODE : TDA1675A

DESCRIPTION

The TDA1675A is a monolithic integrated circuit in 15-lead Multiwatt® package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke of 110° colour TV picture tubes. It offers a wide range of applications also in portable CTVs, B&W TVs, monitors and displays.

PIN CONNECTIONS (top view)



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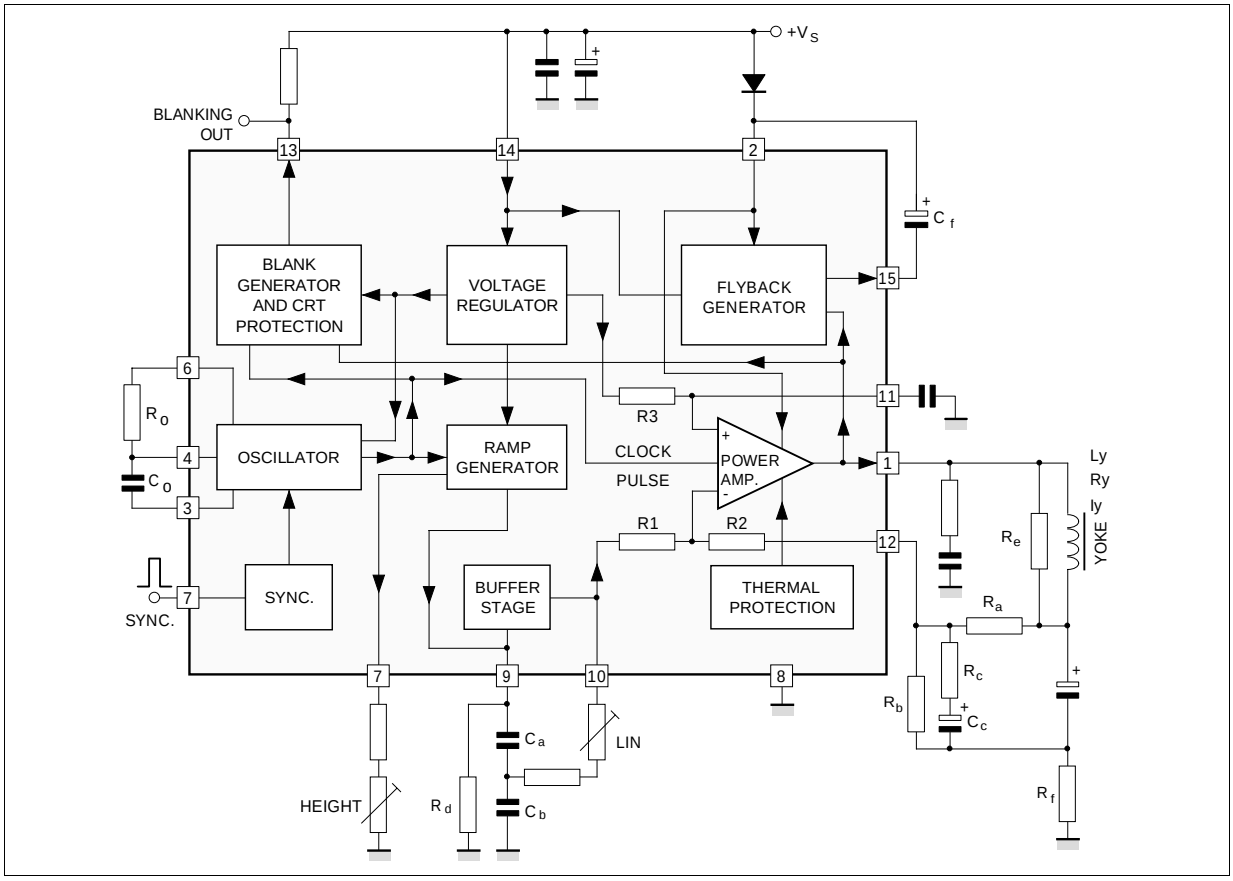
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 14	35	V
V_1, V_2	Flyback Peak Voltage	65	V
V_5	Sync. Input Voltage	20	V
V_{11}, V_{12}	Power Amplifier Input Voltage	V_S - 10	V
V_{13}	Voltage at Pin 13	V_S	
I_O	Output Current (non repetitive) at t = 2ms	3	A
I_O	Output Peak Current at f = 50Hz t > 10µs	2	A
I_O	Output Peak Current at f = 50Hz t ≤ 10 µs	3.5	A
I_{15}	Pin 15 Peak-to-peak Flyback Current at f = 50Hz, tfly ≤ 1.5ms	3	A
I_{15}	Pin 15 D.C. Current at V1 < V_{14}	100	mA
P_{tot}	Maximum Power Dissipation at $T_{case} \leq 60^oC$	30	W
T_{stg}, T_j	Storage and Junction Temperature	- 40, + 150	^oC

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THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max.	3	$^oC/W$
$R_{TH(j-a)}$	Thermal Resistance Junction-ambient	Max.	40	$^oC/W$

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DC ELECTRICAL CHARACTERISTICS (V_S = 35V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 quiescent current	$I_1 = 0$		16	36	mA	1b
$-I_9$	Ramp generator bias current	$V_9 = 0$		0.02	1	µA	1b
$-I_9$	Ramp generator current	$V_9 = 0$; $-I_7 = 20\mu A$	18.5	20	21.5	µA	1b
$\frlvert \Delta I_9 \frrvert / I_9$	Ramp generator non linearity	ΔV_9 = 0 to 15V, $-I_7$ = 20µA		0.2	1	%	1b
I_{14}	Pin 14 quiescent current			25	45	mA	1b
V_1	Quiescent output voltage	V_S = 35V, R_a = 2.2kΩ, R_b = 1kΩ V_S = 15V, R_a = 390Ω, R_b = 1kΩ	16.4 6.9	17.8 7.5	19.5 8.1	V V	1a
V_{1L}	Output saturation voltage to ground	I_1 = 1.2A,		1	1.4	V	1c
V_{1H}	Output saturation voltage to supply	$-I_1$ = 1.2A		1.6	2.2	V	1d
V_4	Oscillator virtual ground			0.45		V	1b
V_7	Regulated voltage at pin 7	$-I_7 = 20\mu A$	6.3	6.6	7	V	1b
$\Delta V_7 / \Delta V_S$	Regulated voltage drift with supply voltage	ΔV_S = 15 to 35V		1	2	mV/V	1b
V_{11}	Amplifier input (+) reference voltage		4.1	4.4	4.7	V	1b
V_{13}	Blanking output saturation voltage	I_{13} = 10 mA		0.35	0.5	V	1a
V_{15}	Pin 15 saturation voltage to ground	I_{15} = 20 mA		1	1.5	V	1a

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Figure 1 : DC Test Circuit.

Figure 1a

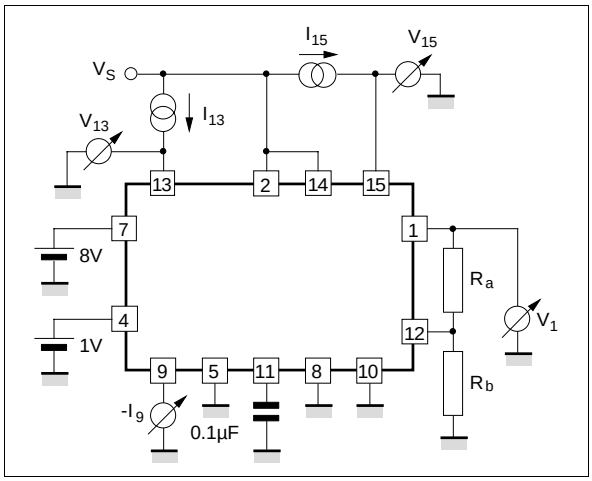

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Figure 1b

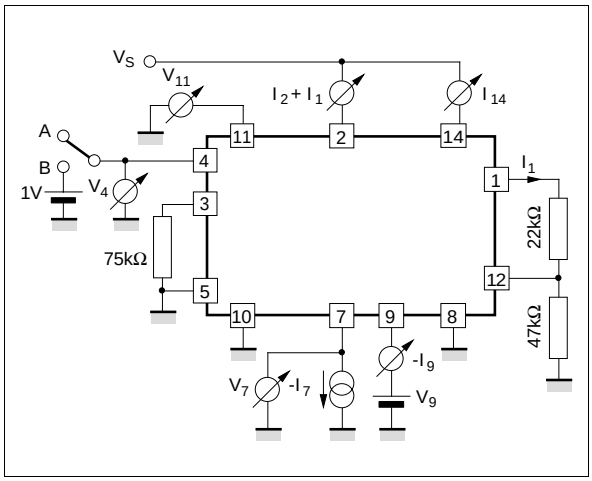

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Figure 1c

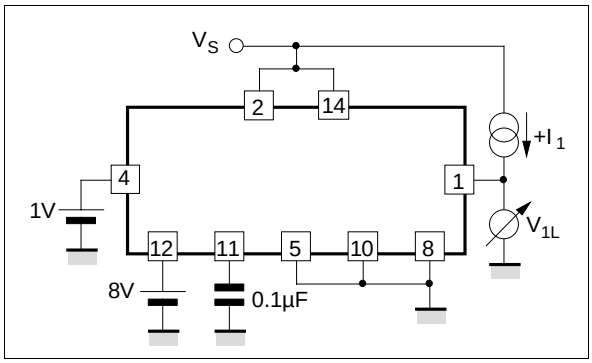

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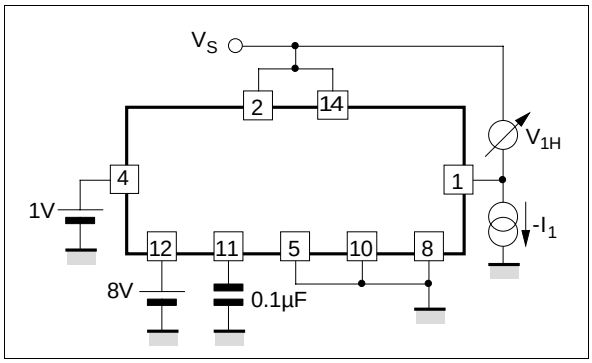
Figure 1d



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AC ELECTRICAL CHARACTERISTICS

(Refer to A.C. test circuit of fig. 2, T_{amb} = 25°C, V_S = 24V, f = 50Hz, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply Current	$I_Y = 2A_{PP}$		295		mA
I_5	Sync Input Current Required to Sync		100			µA
V_1	Flyback Voltage	I_y = 2App		50		V
V_3	Peak-to-peak Oscillator Sawtooth Voltage	I_5 = 0 I_5 = 100µA		3.6 3.4		V V
$V_{10TH(L)}$	Start Scan Level of the Input Ramp			1.85		V
t_{FLY}	Flyback Time	Iy = 2App		0.6		ms
t_{BLANK}	Blanking Pulse Duration	f_o = 50Hz, T_j = 75°C f_o = 60Hz, T_j = 75°C	1.33	1.4 1.17	1.47	ms ms
f_o	Free Running Frequency	R_o = 7.5kΩ, C_o = 330nF, T_j = 75°C R_o = 6.2kΩ, C_o = 330nF, T_j = 75°C	42	43.5 52.5	46	Hz Hz
Δf	Synchronization Range	I_5 = 100µA, T_j = 75°C	14	16		Hz
T_j	Junction Temperature for Thermal Shut-down			145		°C
V_{ON}	Peak-to-peak Output Noise				35	mV_{PP}

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Figure 2 : AC Test Circuit

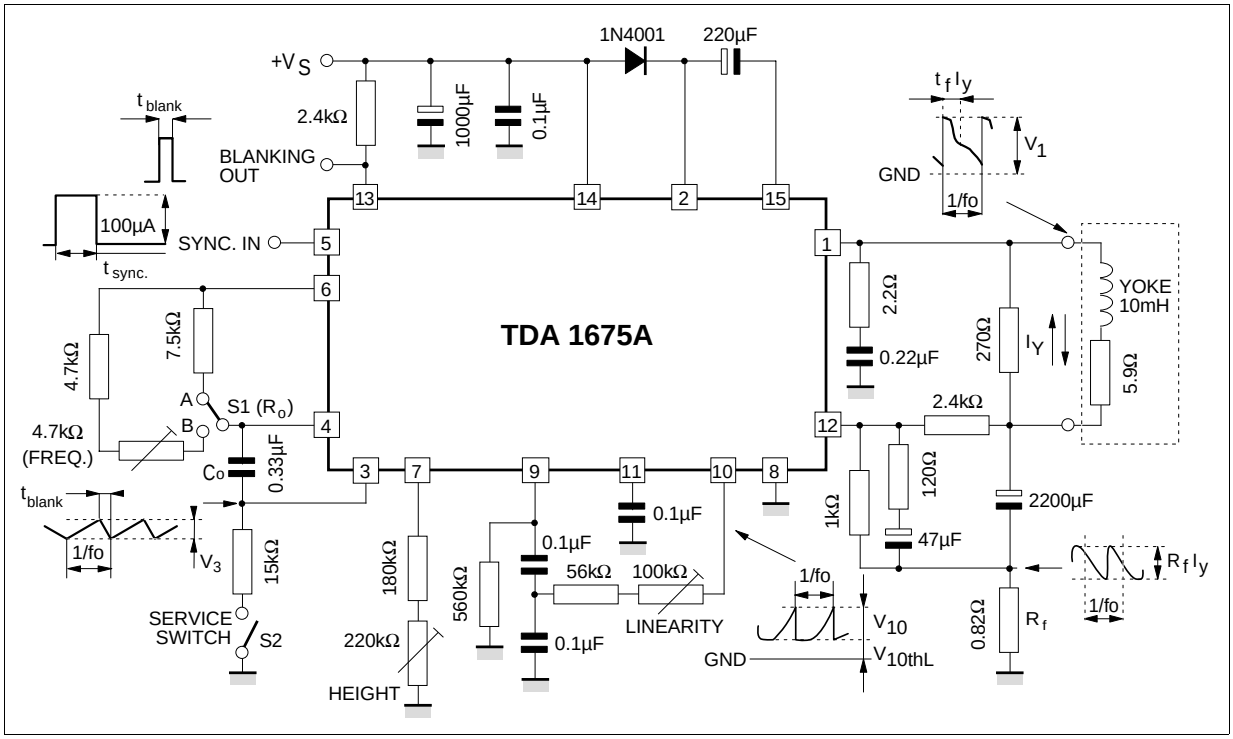
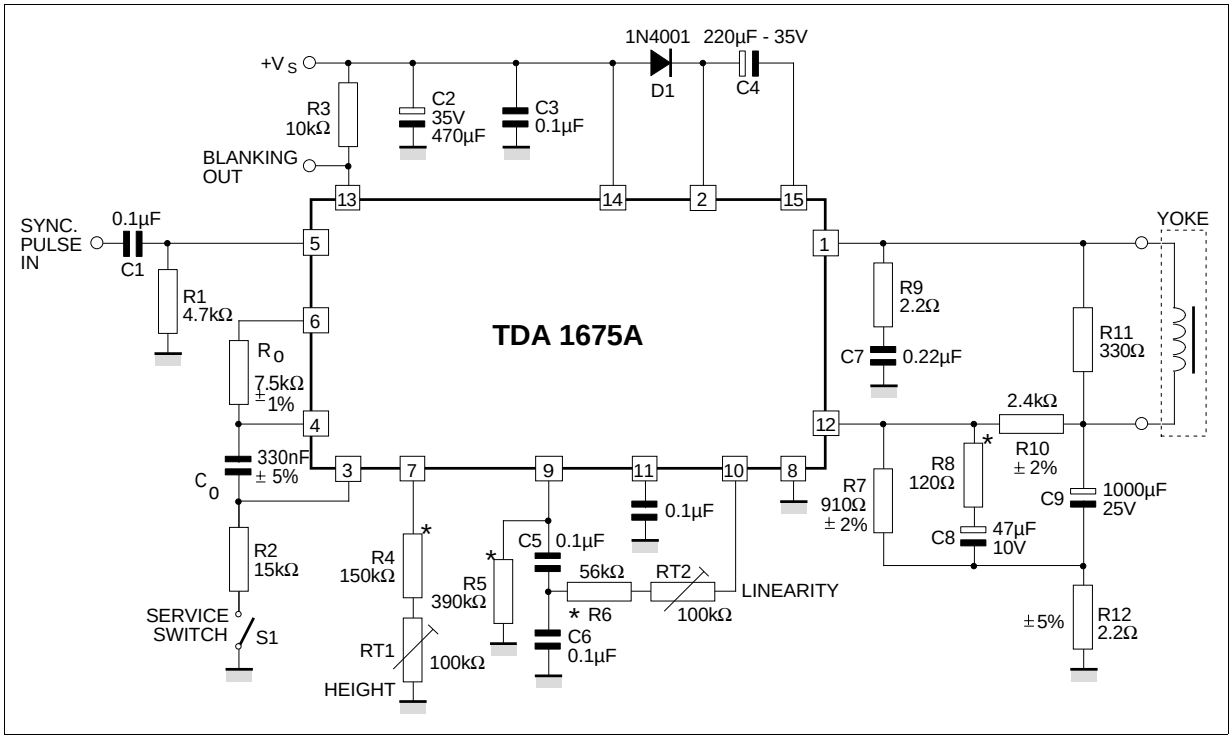


Figure 3 : Application Circuit for Small Scree 90° CTV Set (R_y = 15Ω ; L_y = 30 mH ; I_y = 0.82 A_{PP})



* The value depends on the characteristics of the CRT. The value shown is indicative only.

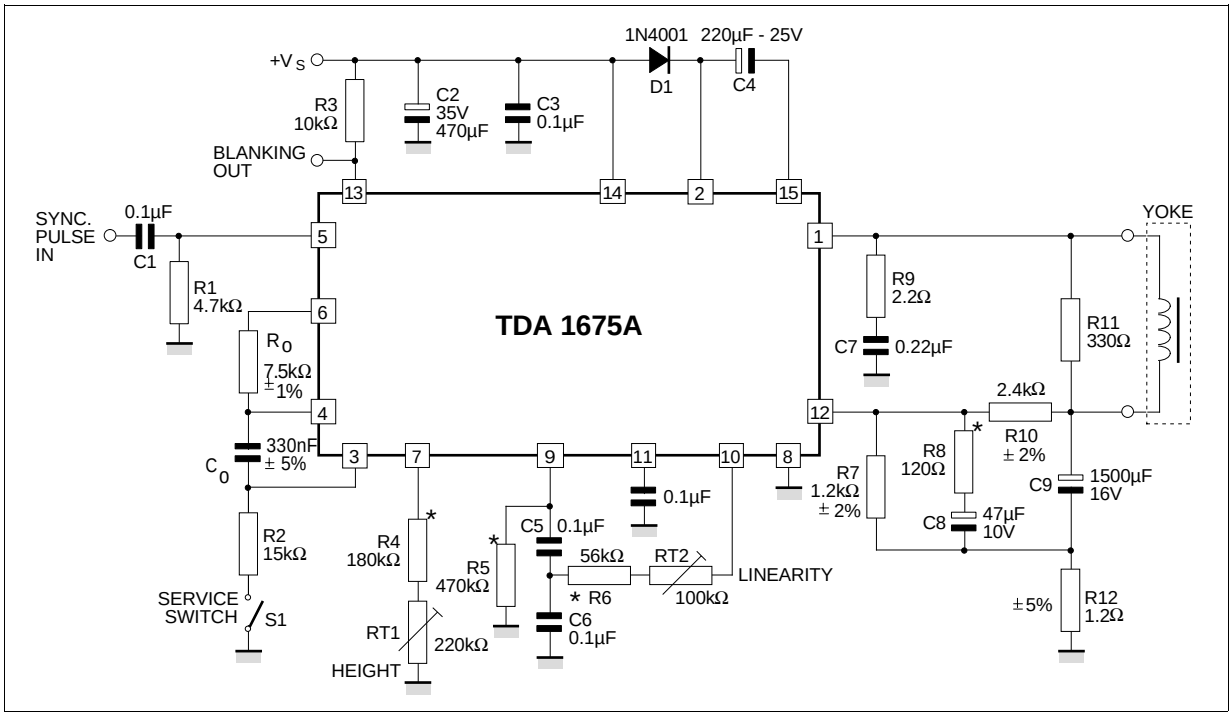
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	25	V
I_S	Supply current	140	mA
t_{FLY}	Flyback time	0.7	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	2.4	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for T_{amb} = 60°C and $T_{j\,max}$ = 110°C for T_{amb} = 60°C and $T_{j\,max}$ = 120°C	 13 16	 °C/W °C/W

1675A-05.TBL

* Worst case condition.

Figure 4 : Application Circuit for 110° CTV Set (R_y = 9.6Ω ; L_y = 24.6 mH ; I_y = 1.2 A_{PP})



* The value depends on the characteristics of the CRT. The value shown is indicative only.

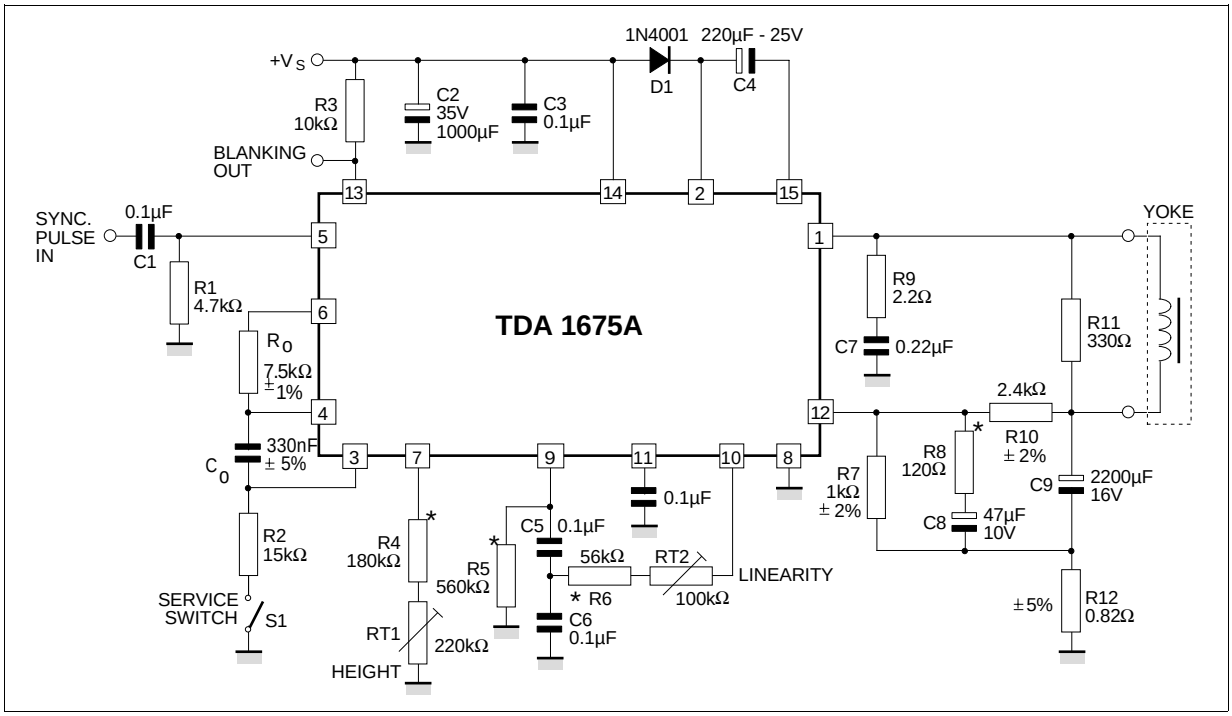
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	22.5	V
I_S	Supply current	185	mA
t_{FLY}	Flyback time	1	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	2.7	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for Tamb = 60°C and $T_{j\,max}$ = 110°C for T_{amb} = 60°C and $T_{j\,max}$ = 120°C	 11.5 14.5	 °C/W °C/W

1675A-06.TBL

* Worst case condition.

Figure 5 : Application Circuit for 110° CTV Set (R_y = 5.9Ω ; L_y = 10 mH ; I_y = 1.95 A_{PP})



* The value depends on the characteristics of the CRT. The value shown is indicative only.

TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	24	V
I_S	Supply current	285	mA
t_{FLY}	Flyback time	0.6	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	4.3	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for Tamb = 60°C and $T_{j\,max}$ = 110°C for T_{amb} = 60°C and $T_{j\,max}$ = 120°C	 6.5 8.5	 °C/W °C/W

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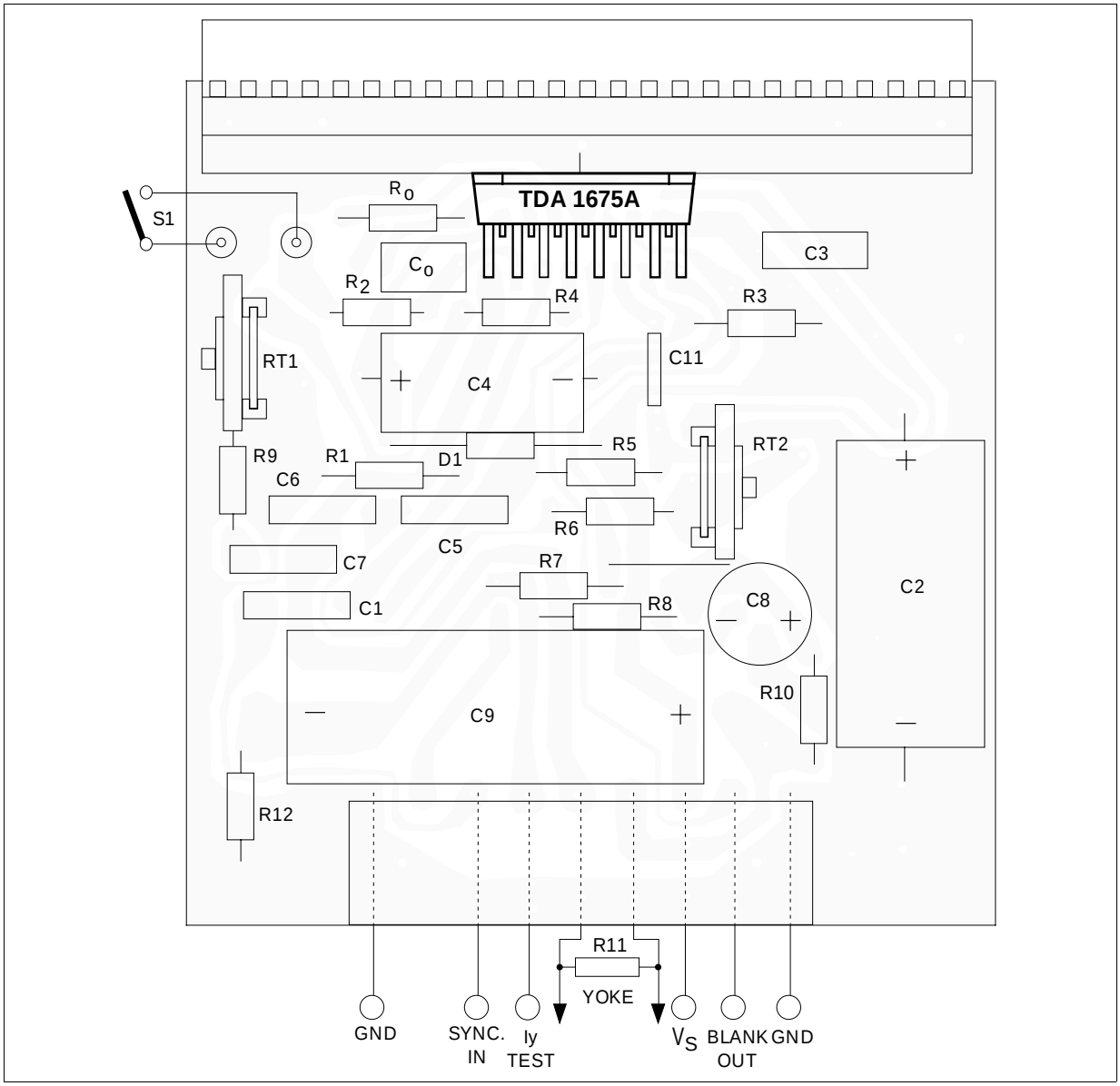
* Worst case condition.

Figure 6 : PC Board and Components Layout for the Application Circuits of Figures 3, 4 and 5 (1 : 1 scale)



APPLICATION INFORMATION (Refer to the block diagram)

Oscillator and sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches R_o high or low so allowing the charge or the discharge of C_o under constant current conditions.

The Sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

Pin 4 is the inverting input of the amplifier used as integrator.

Pin 6 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.

Pin 3 is the output of the amplifier.

Pin 5 is the input for sync pulses (positive)

Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.

The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor a new voltage ramp is immediately allowed.