

SANYO

No.3042

LC7821N,7822N,7823N

CMOS LSI

Analog Function Switch

Use

- Serial data-controlled function select switch suited for use in amplifiers, receivers.

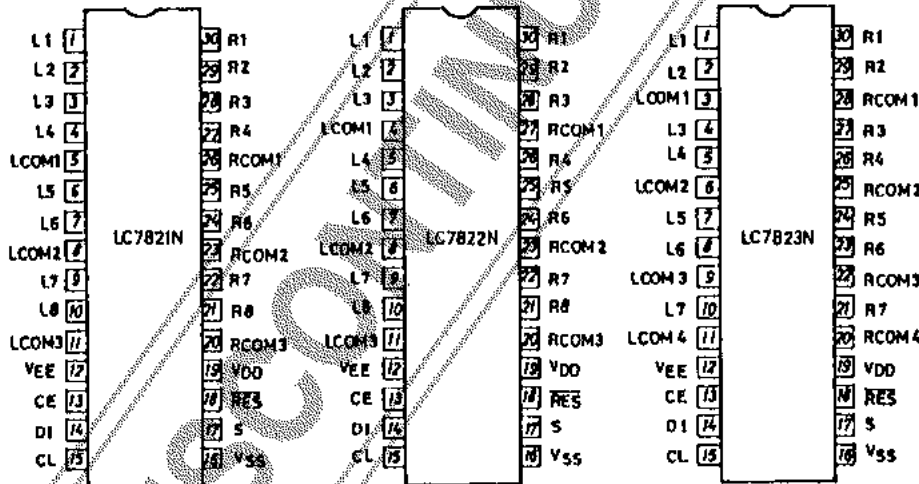
Features

- Analog switches of 8 channels \times 2 (LC7823N : 7 channels \times 2) are contained. Three types are available according to the internal connection.
- Control is exercised by serial data. The LC7821N,7822N,7823N may be interfaced with a microcomputer (5V supply) easily.
- Even if two ICs of the same type are used, they may be connected to the common bus line because the S (selector) pin is provided.
- Reset pin used to turn OFF all analog switches
- Wide dynamic range because of $\pm 20V$ breakdown voltage

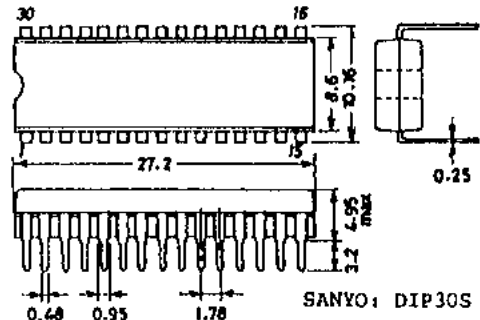
Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	V _{DD} max	V _{DD} -0.3 to +20	V
	V _{EE} max	V _{EE} -20 to +0.3	V
Maximum Input Voltage	V _{I1}	D1, CL, CE, S, RES	-0.3 to +20
	V _{I2}	L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	V _{EE} -0.3 to V _{DD} +0.3
Analog Switch ON-State Voltage Difference	ΔV_{ON}	Switch ON	0.5 V
Allowable Power Dissipation	P _d max	Ta \leq 75°C	100 mW
Operating Temperature	T _{opg}		-30 to +75 °C
Storage Temperature	T _{stg}		-40 to +125 °C

Pin Assignment



Case Outline 3047A-D30SIC
(unit : mm)



The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass-produced. The information herein is believed to be accurate and reliable. However, no responsibility is assumed by SANYO for its use; nor for any infringements of patents or other rights of third parties which may result from its use.

Specifications and information herein are subject to change without notice.

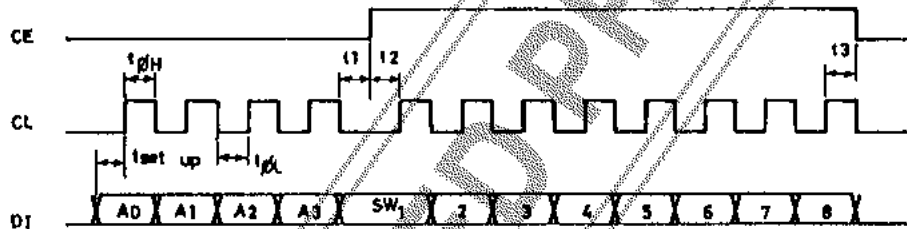
SANYO Electric Co., Ltd. Semiconductor Overseas Marketing Div.
Natsume Bldg. 18-6, 2 chome, Yushima, Bunkyo-ku, TOKYO 113 JAPAN

2109YT, TS No.3042-1/6

LC7821N,7822N,7823N

Allowable Operating Conditions at $T_a = 25^\circ\text{C}, V_{SS} = 0\text{V}, V_{DD} \geq V_{EE} $			min	typ	max	unit
Maximum Supply Voltage	V_{DD}	$V_{DD} - V_{EE} \geq 12\text{V} : V_{DD}$	6.0		18.5	V
	V_{EE}	$V_{DD} - V_{EE} \geq 12\text{V} : V_{EE}$	-18.5		0	V
Input "H"-Level Voltage	V_{IH1}	DI, CL, CE, S	4.0		18.5	V
	V_{IH2}	RES	$0.7V_{DD}$		V_{DD}	V
Input "L"-Level Voltage	V_{IL1}	DI, CL, CE, S	0		0.7	V
	V_{IL2}	RES	0	$0.3V_{DD}$		V
(Analog Switch Input Voltage Range	V_{IN}	L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	V_{EE}		V_{DD}	V
"L"-Level Clock Pulse Width	$t_{\phi L}$	CL	0.5			μsec
"H"-Level Clock Pulse Width	$t_{\phi H}$	CL	0.5			μsec
Setup Time	t_{setup}	CL, DI	0.5			μsec
	t_1^*	CL, CE	0.5			μsec
	t_2^*	CL, CE	0.5			μsec
	t_3^*	CL, CE	0.5			μsec
	Reset Minimum Pulse Width	t_{wRES}	$V_{DD} \geq 6\text{V} : \overline{\text{RES}}$	1.0		
Hysteresis Width	V_{H1}	CL, CE, DI	0.3			V

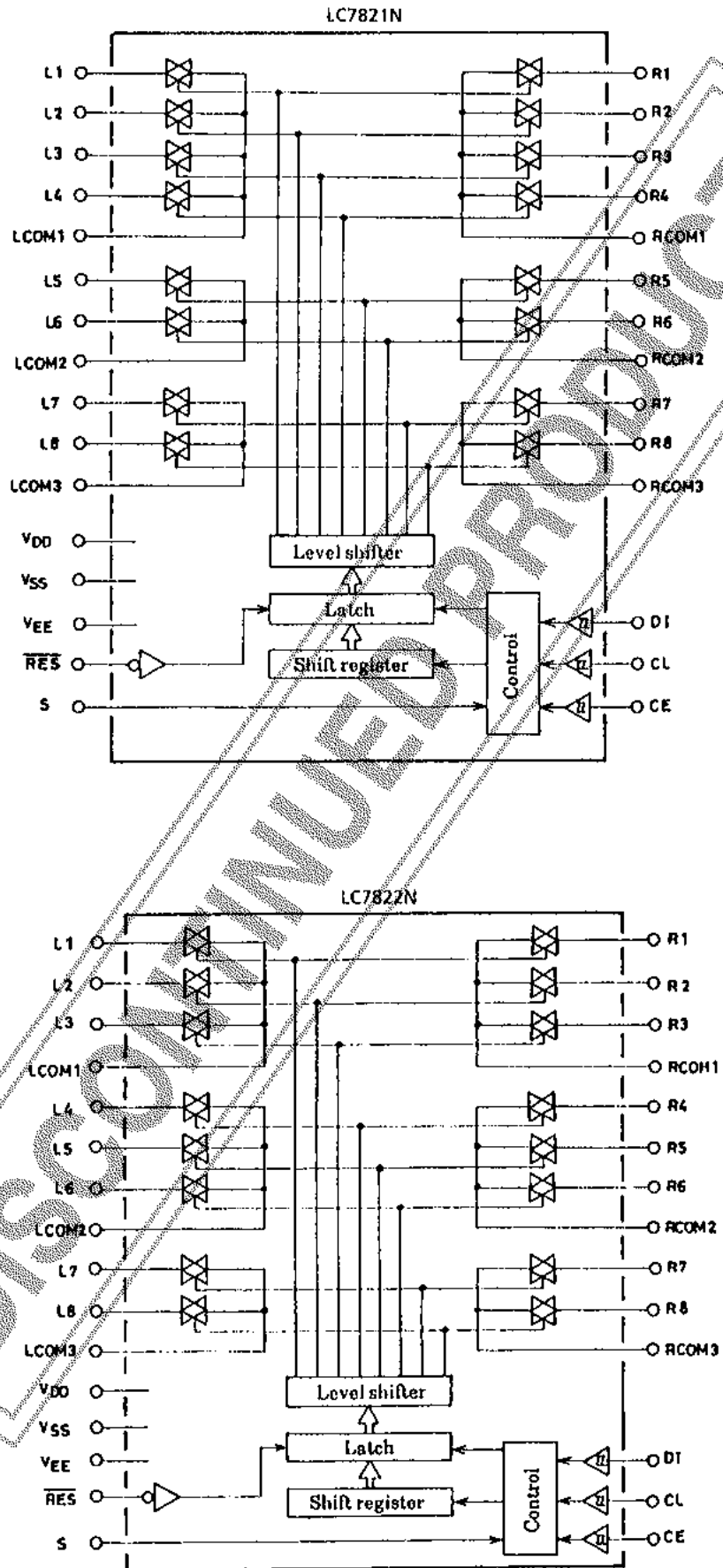
* : CE, CL, DI waveforms



Electrical Characteristics at $T_a = 25^\circ\text{C}, V_{SS} = 0\text{V}$			min	typ	max	unit
Analog Switch ON-State Resistance	R_{ON1}	$I = 1\text{mA}, V_{DD} - V_{EE} = 12\text{V} : L1 \text{ to } L8, R1 \text{ to } R8, LCOM1 \text{ to } LCOM4, RCOM1 \text{ to } RCOM4$		150		Ω
	R_{ON2}	$I = 1\text{mA}, V_{DD} - V_{EE} = 37\text{V} : L1 \text{ to } L8, R1 \text{ to } R8, LCOM1 \text{ to } LCOM4, RCOM1 \text{ to } RCOM4$		70		Ω
Total Harmonic Distortion	THD1	$V_{IN} = 1\text{V}_{\text{rms}}, f = 1\text{kHz}, V_{DD} - V_{EE} = 37\text{V} : L1 \text{ to } L8, R1 \text{ to } R8, LCOM1 \text{ to } LCOM4, RCOM1 \text{ to } RCOM4$		0.0015	0.01	%
	THD2	$V_{IN} = 0.1\text{V}_{\text{rms}}, f = 1\text{kHz}, V_{DD} - V_{EE} = 37\text{V} : L1 \text{ to } L8, R1 \text{ to } R8, LCOM1 \text{ to } LCOM4, RCOM1 \text{ to } RCOM4$		0.01	0.05	%
Feedthrough	F_{TH}	$V_{IN} = 0\text{dBV}, f = 10\text{kHz}, V_{DD} - V_{EE} = 37\text{V} : L1 \text{ to } L8, R1 \text{ to } R8, LCOM1 \text{ to } LCOM4, RCOM1 \text{ to } RCOM4$		65		dB
Crosstalk	CT	$V_{IN} = 0\text{dBV}, f = 10\text{kHz}, V_{DD} - V_{EE} = 37\text{V} : L1 \text{ to } L8, R1 \text{ to } R8, LCOM1 \text{ to } LCOM4, RCOM1 \text{ to } RCOM4$		75		dB
Input "H"-Level Current	I_{IH}	$V_I = 18.5\text{V} : DI, CL, CE, S, \overline{\text{RES}}$			10	μA
Input "L"-Level Current	I_{IL}	$V_I = 0\text{V} : DI, CL, CE, S, \overline{\text{RES}}$	-10			μA
(Analog Switch OFF-State Leakage Current	I_{OFF}	$V_I = V_{EE} \text{ to } V_{EE} + 37\text{V} : L1 \text{ to } L8, R1 \text{ to } R8, LCOM1 \text{ to } LCOM4, RCOM1 \text{ to } RCOM4$	-10		10	μA
Current Dissipation	I_{DD}	V_{DD}			1.0	mA

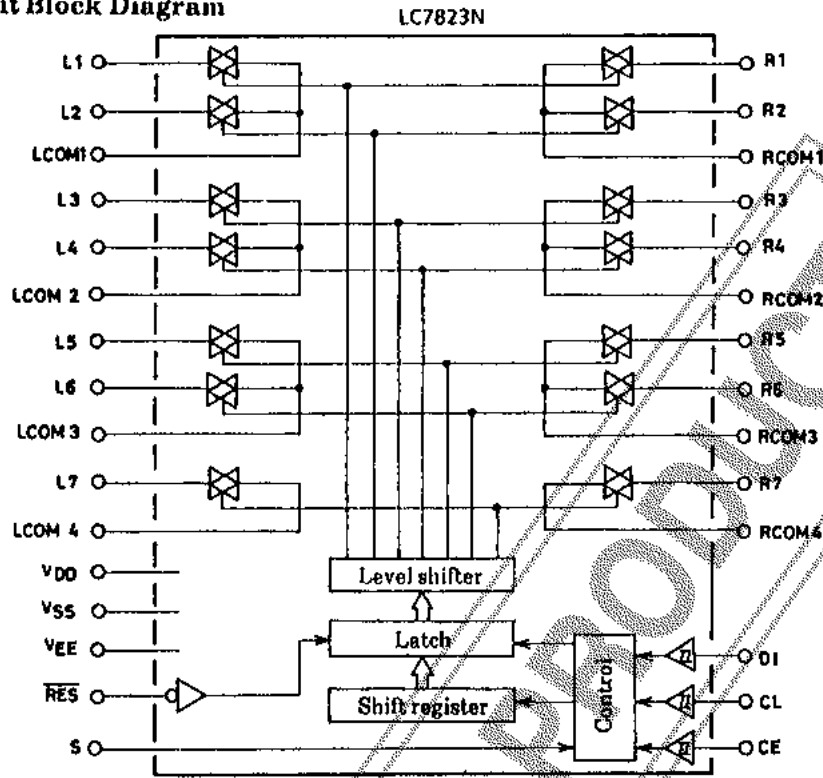
LC7821N,7822N,7823N

Equivalent Circuit Block Diagram



LC7821N,7822N,7823N

Equivalent Circuit Block Diagram



Pin Description

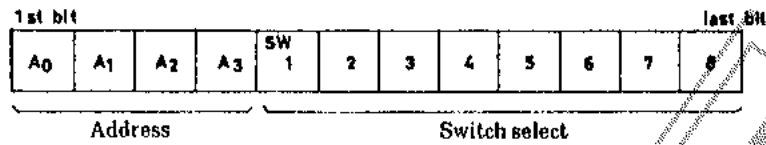
Pin Name	I/O	Internal Equivalent Circuit	Function																																											
V _{DD} , V _{SS} , V _{EE}			Power supply pins																																											
L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		See Block Diagram.	Input/output pins for analog switches.																																											
CL, DI, CE	I		Serial data input pins (Schmitt buffer) CL---Clock input pin DI---Data input pin CE---Chip enable pin																																											
S	I		Select pin in the two ICs-used mode When the S pin is brought to "L" or "H" level, the address will become as shown below. <table border="1"> <thead> <tr> <th rowspan="2">Type No.</th> <th rowspan="2">S Pin</th> <th colspan="4">Address</th> </tr> <tr> <th>A0</th> <th>A1</th> <th>A2</th> <th>A3</th> </tr> </thead> <tbody> <tr> <td rowspan="2">LC7821N</td> <td>L</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>H</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td rowspan="2">LC7822N</td> <td>L</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>H</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td rowspan="2">LC7823N</td> <td>L</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>H</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Type No.	S Pin	Address				A0	A1	A2	A3	LC7821N	L	0	1	0	1	H	1	1	0	1	LC7822N	L	0	0	1	1	H	1	0	1	1	LC7823N	L	0	1	1	1	H	1	1	1	1
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$\overline{\text{RES}}$	I		Reset pin When power is applied, the state of the analog switches will be indeterminate. When this pin is brought to "L" level, all analog switches will be turned OFF.																																											

LC7821N,7822N,7823N

Operation Description

1. Data input method

The LC7821N,7822N,7823N are controlled by inputting serial data to the CI, DI, CE pins. Data consists of 12bits in all (address : 4 bits, data : 8 bits).



Each switch No. corresponds to analog switches L1 to L8, R1 to R8.
Set the bit of a switch to be turned ON to 1.

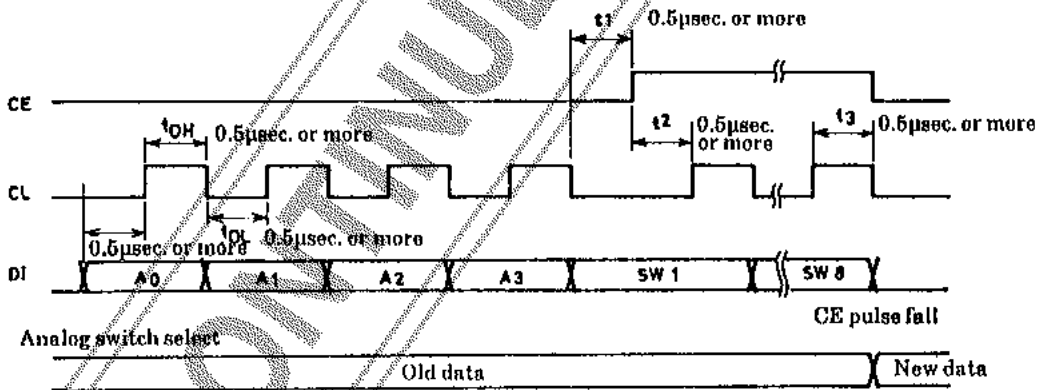
0 ----- OFF
1 ----- ON

The address is used for chip select when connected to the common bus line.
When the S pin is brought to "L" or "H" level, the transmit data will become as shown below.

Type No.	S Pin	Address			
		A0	A1	A2	A3
LC7821N	L	0	1	0	1
	H	1	1	0	1
LC7822N	L	0	0	1	1
	H	1	0	1	1
LC7823N	L	0	1	1	1
	H	1	1	1	1

Note : For the LC7823N, the bit of switch 8 becomes "don't care" (0 or 1).
The reason for this is that the LC7823N contains 7 channels × 2 of analog switches.

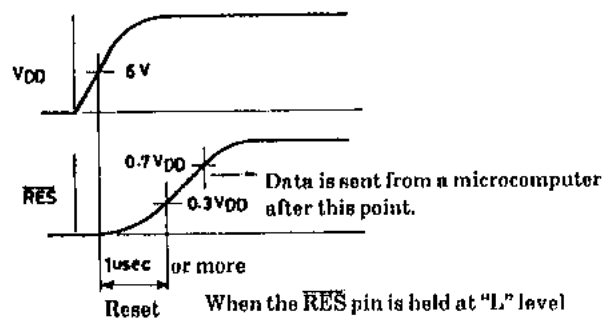
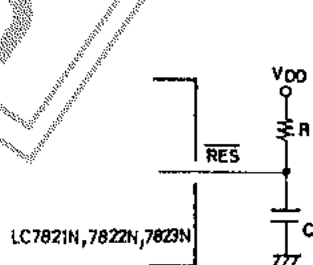
2. Timing of DI,CI,CE pulse signals



Data is fetched into the inside on the positive transition of the CL pulse and latched on the negative transition of the CE pulse.

3. Reset pin

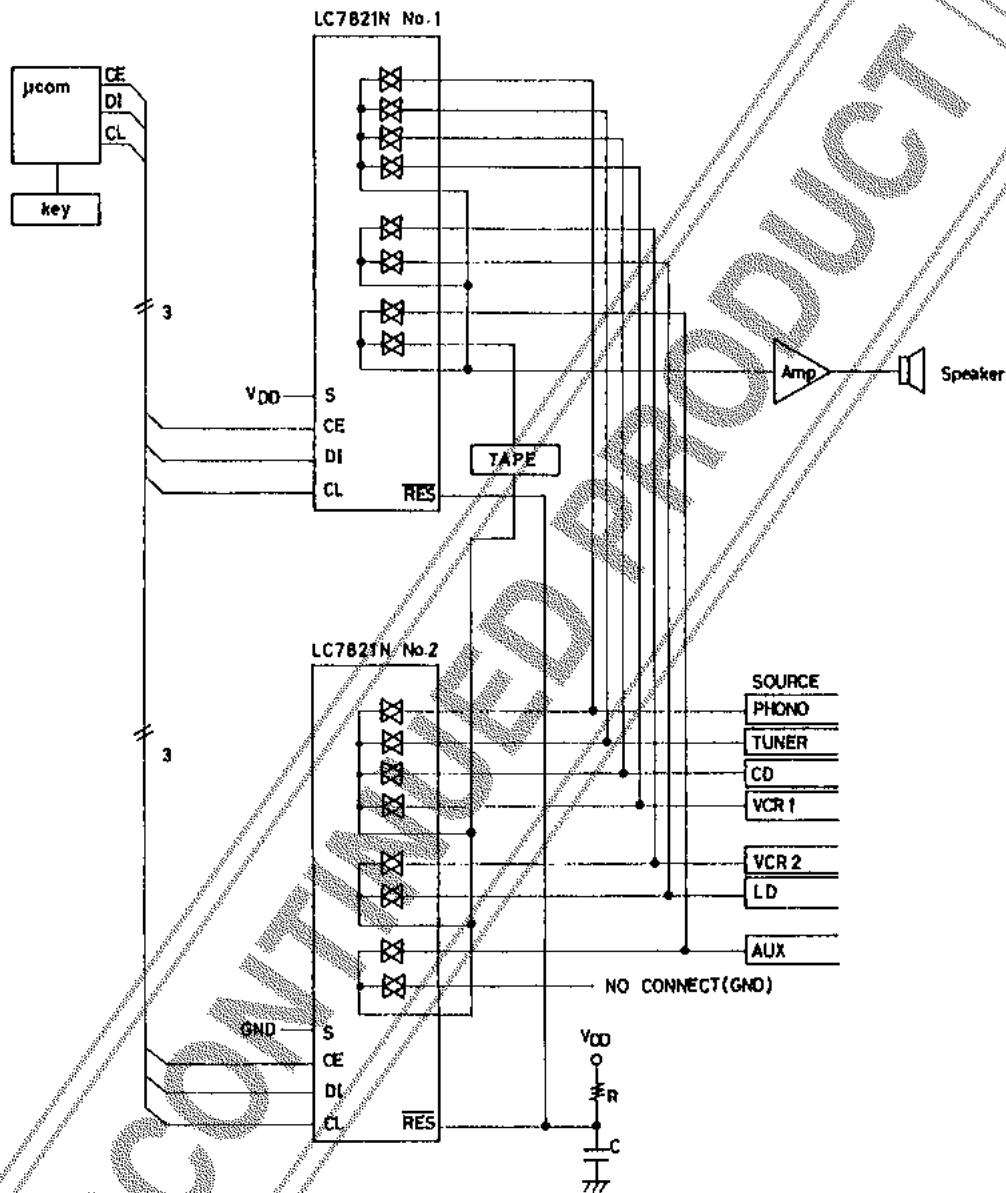
When power is applied, the state of the analog switches will be indeterminate. All analog switches may be turned OFF by connecting C, R to this pin externally.



When the RES pin is held at "L" level for 1µsec. or more, all analog switches will be turned OFF.

- When the C²B is shared by plural ICs :
The state of the LC7821N,7822N,7823N remains unchanged until they receive the address data assigned to them.

Sample Application Circuit



Note) The other channel also has the same connection.